

FIGURE 1

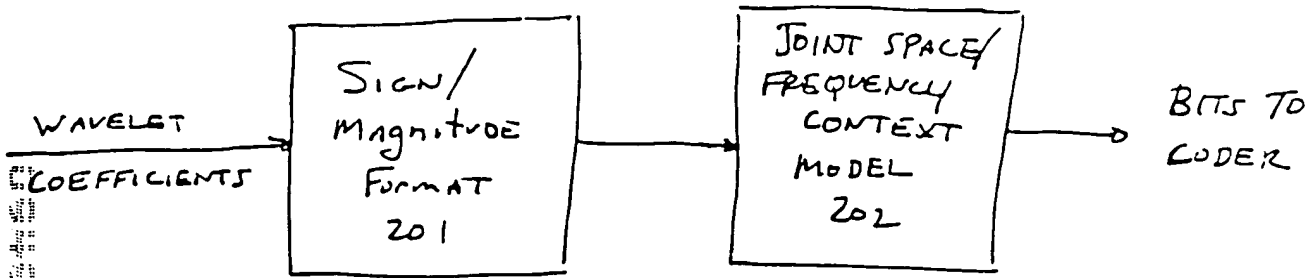


Figure 2

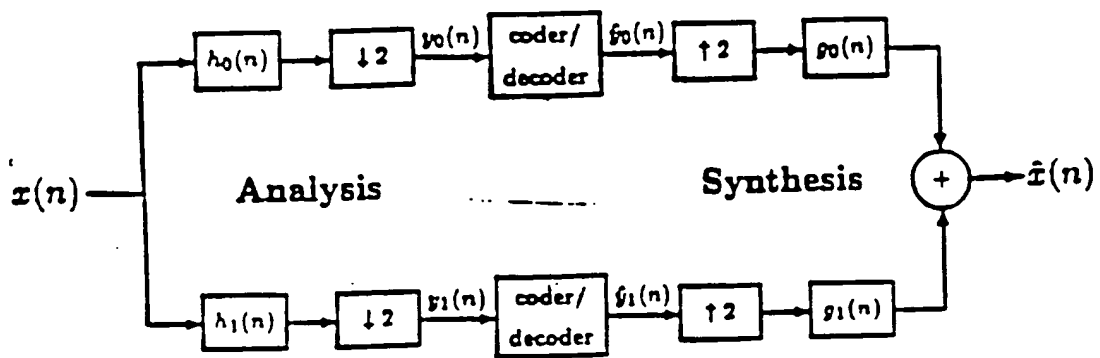
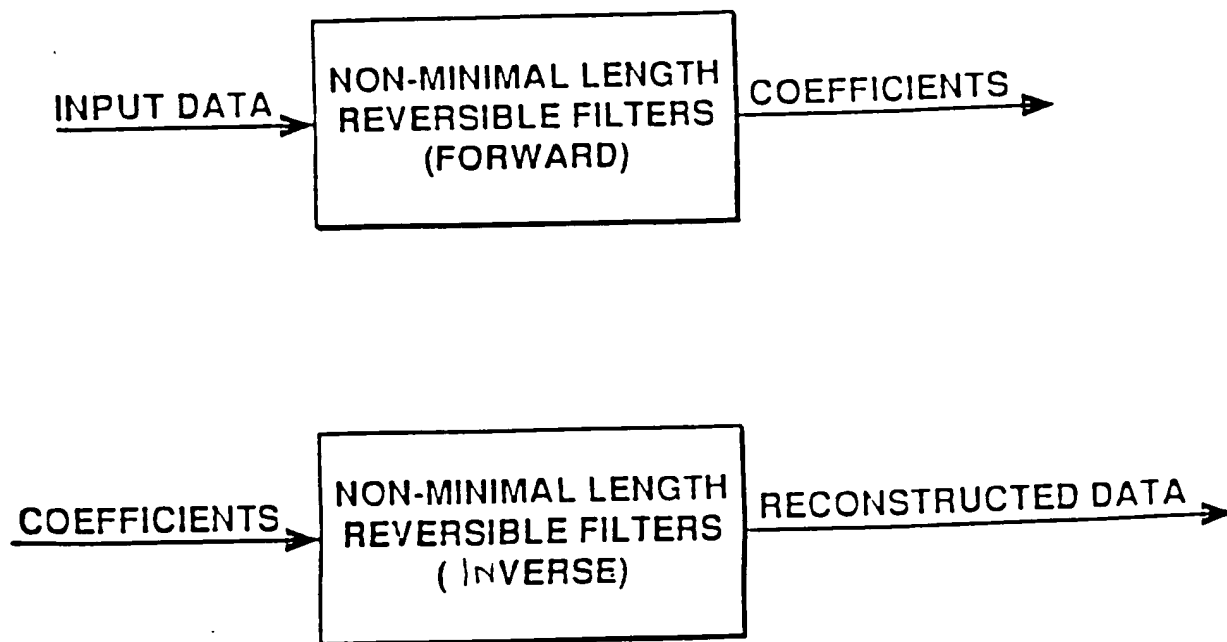


FIGURE 3A



*Figure 38*

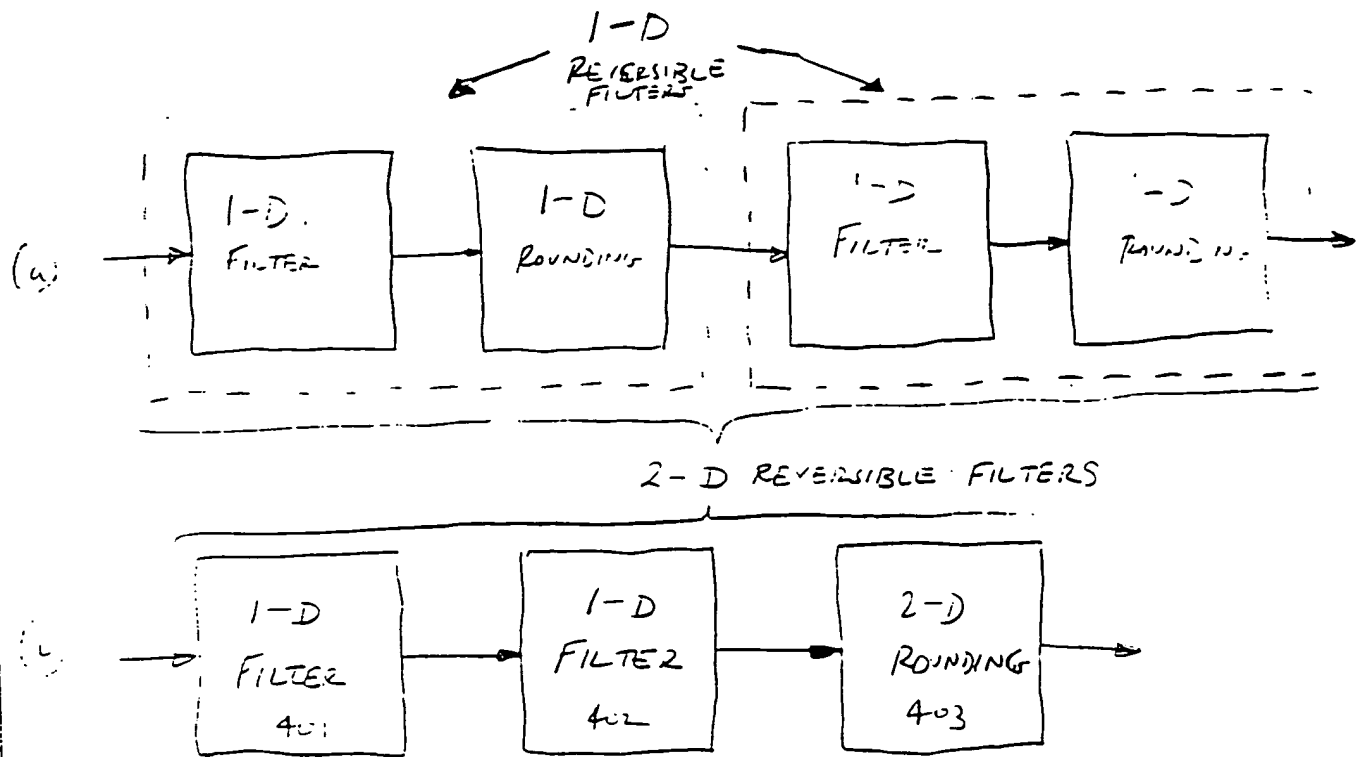


Figure 4

ORIGINAL IMAGE

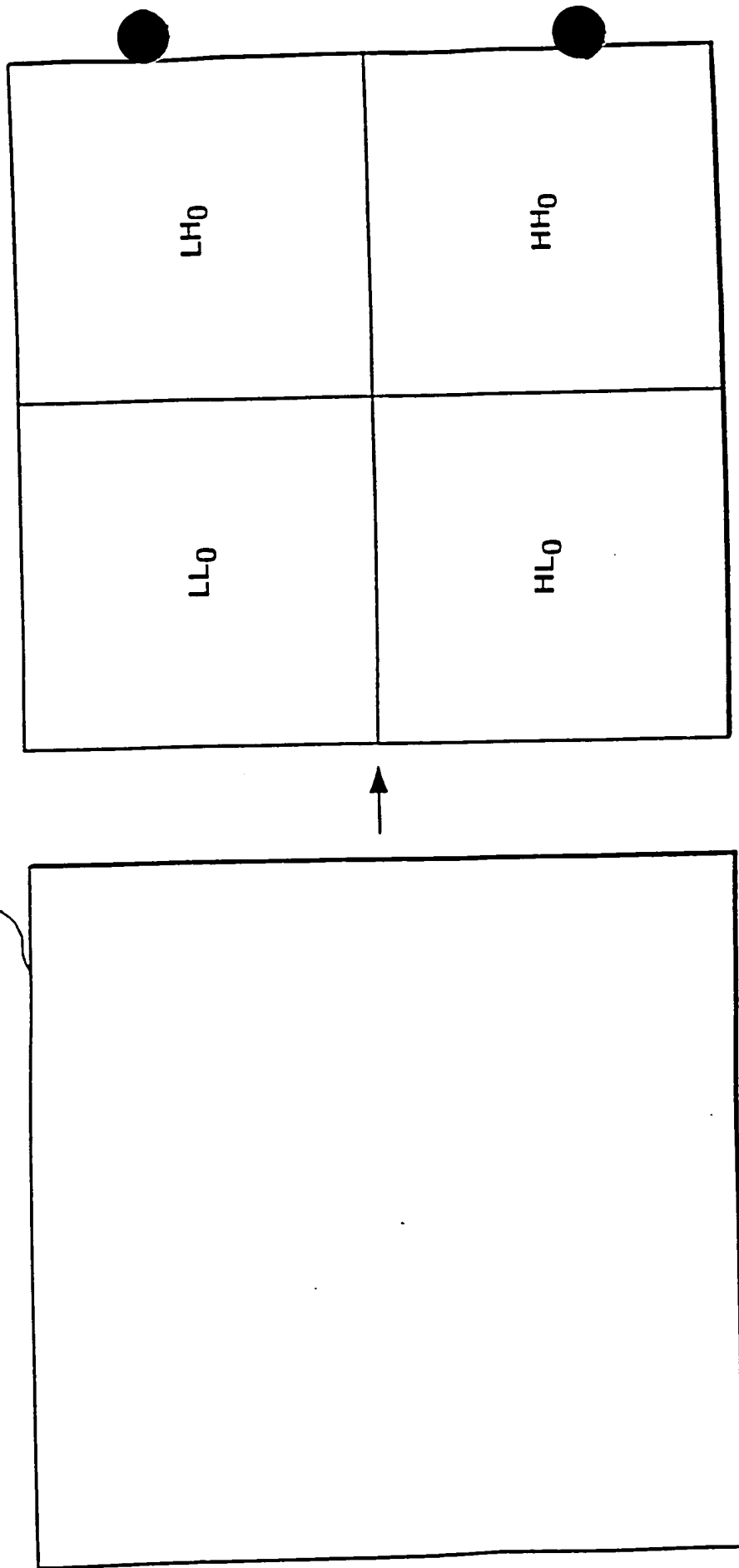
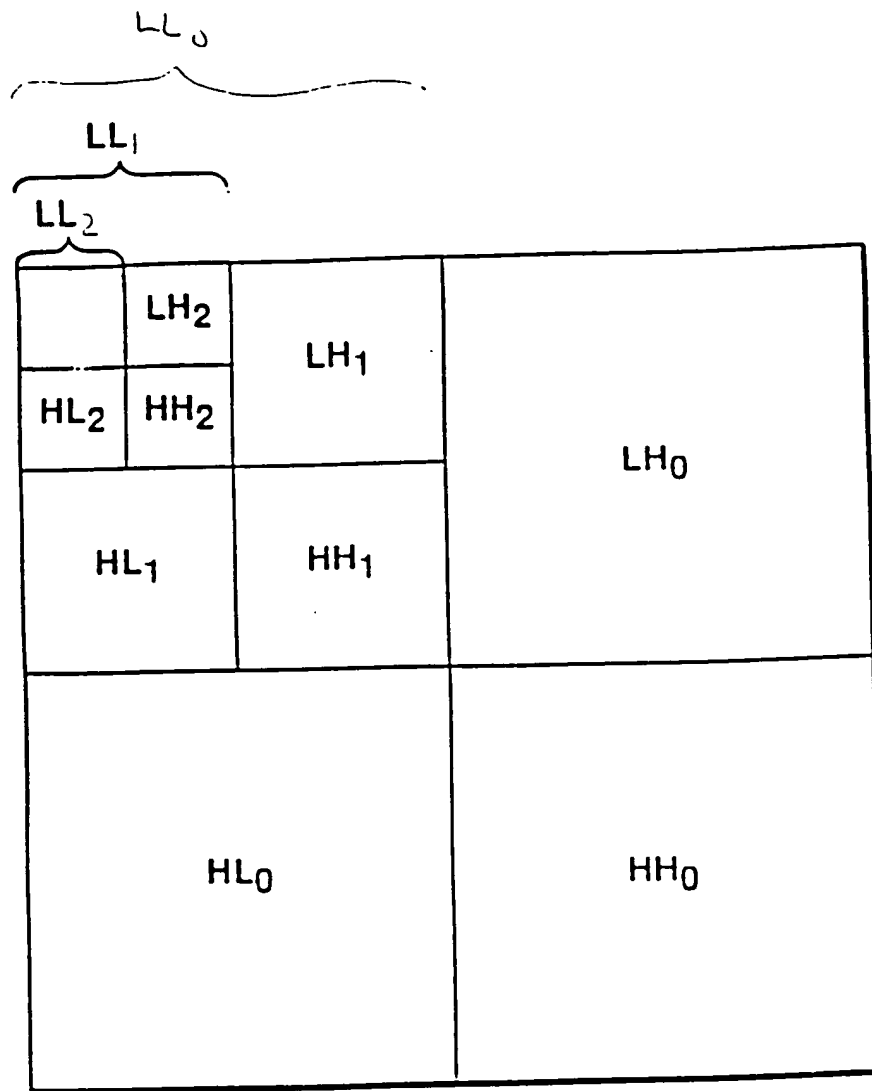


Figure 5A

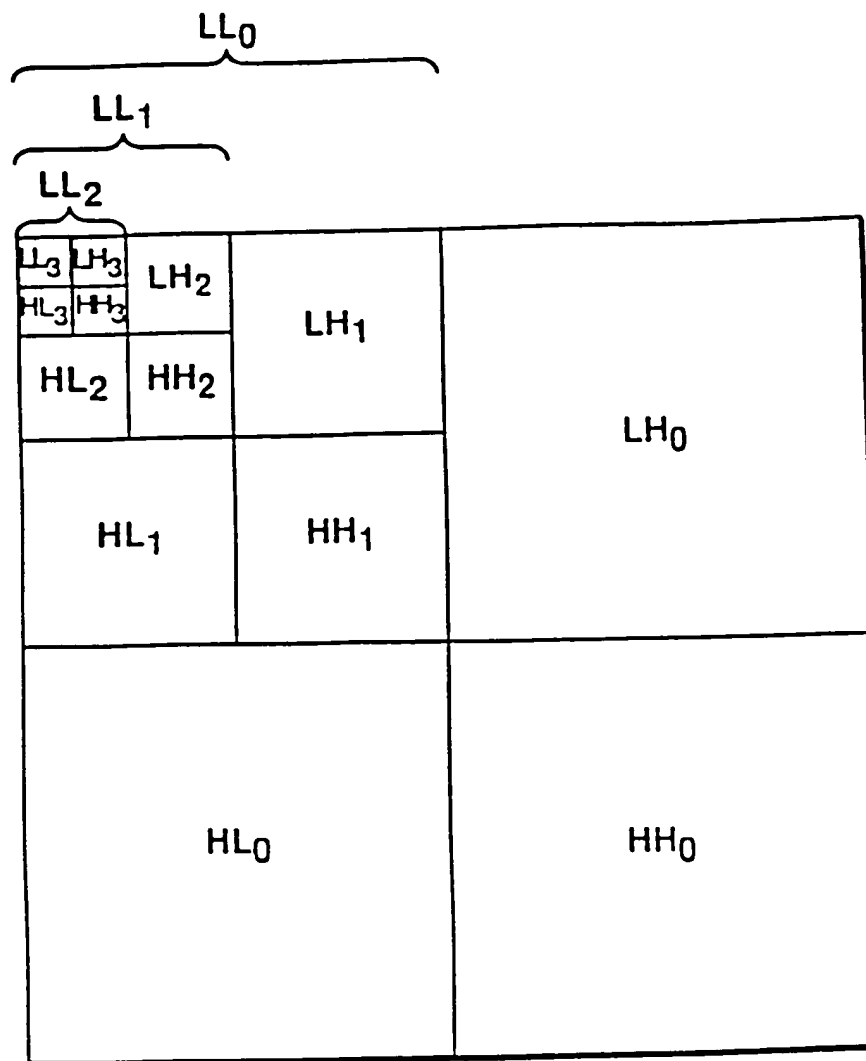
LL <sub>1</sub>	LH <sub>1</sub>	LH <sub>0</sub>
HL <sub>1</sub>	HH <sub>1</sub>	
HL <sub>0</sub>		HH <sub>0</sub>

*Figure 5B*



*Figure 5 C*





**Figure 5D**

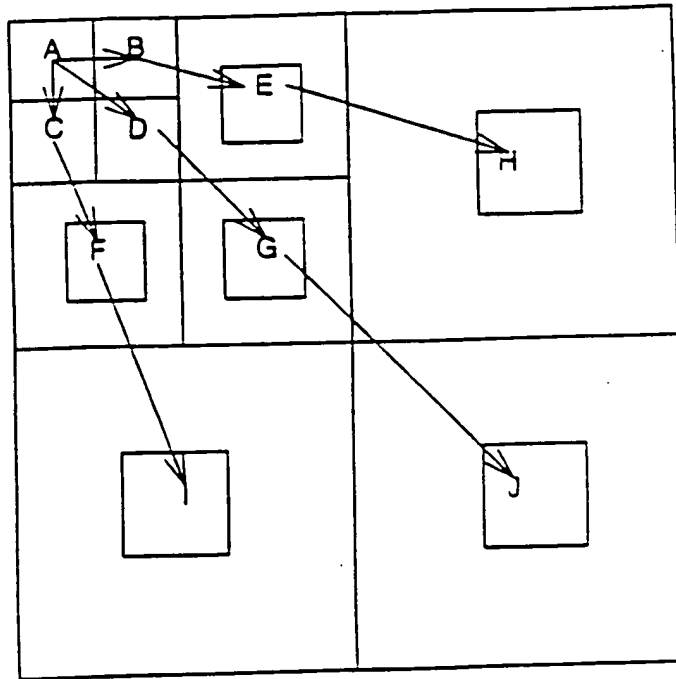


Figure 6

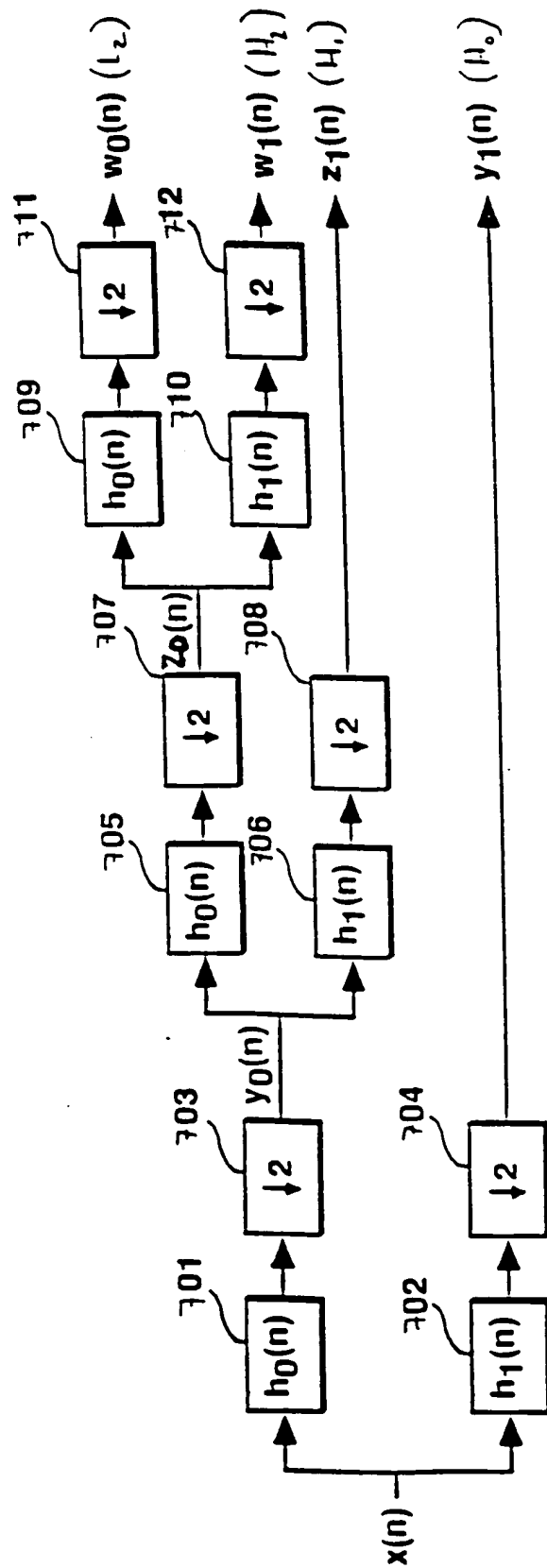


Figure 8 is a block diagram of a hierarchical structure. The diagram shows a series of blocks labeled  $h_0$ ,  $h_1$ , and  $\downarrow 2$  arranged in a tree-like structure. The blocks are connected by arrows, indicating a flow from left to right. The structure is divided into three main sections: HORIZONTAL, VERTICAL, and HORIZONTAL. The HORIZONTAL sections are at the top and bottom, while the VERTICAL section is in the middle. The HORIZONTAL sections consist of blocks labeled  $h_0$  and  $h_1$ , followed by a block labeled  $\downarrow 2$ . The VERTICAL section consists of blocks labeled  $h_0$  and  $h_1$ , followed by a block labeled  $\downarrow 2$ . The diagram shows a flow from left to right, with arrows indicating the direction of the flow. The flow starts from the left, goes through the HORIZONTAL section, then the VERTICAL section, and finally the HORIZONTAL section again. The flow ends at the rightmost block, which is labeled  $h_1$ .

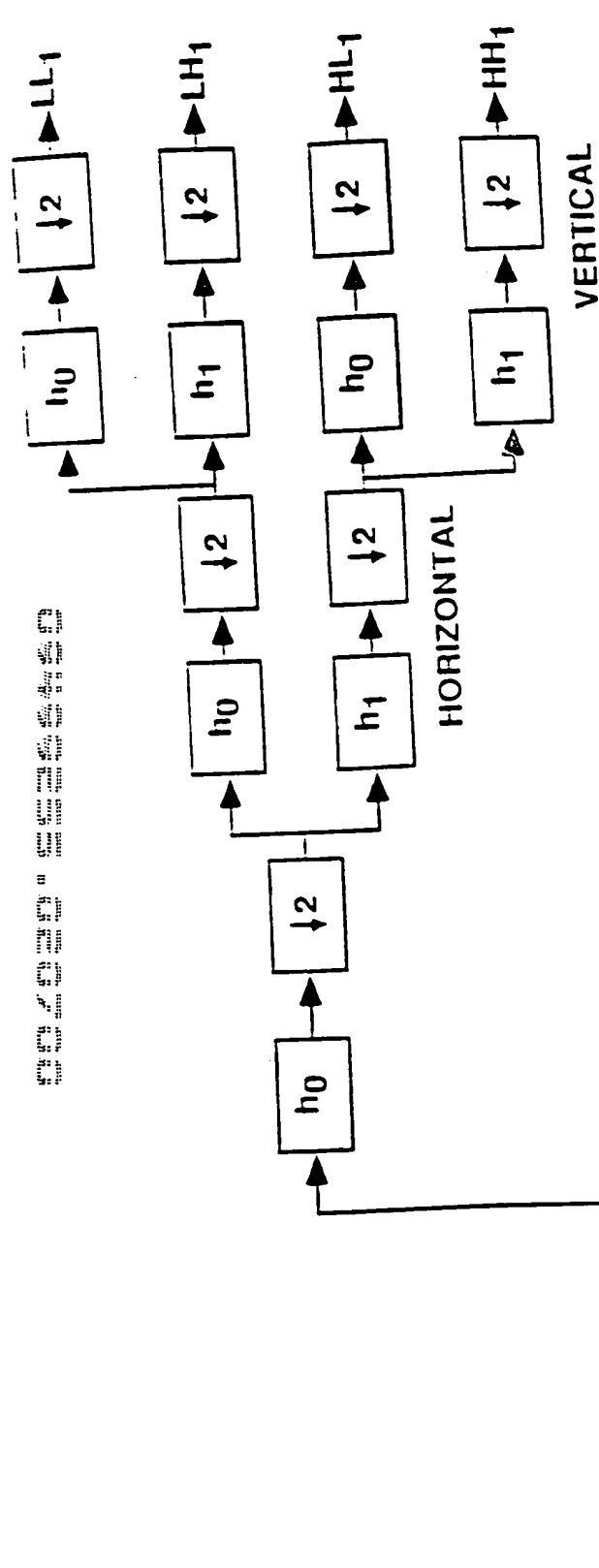
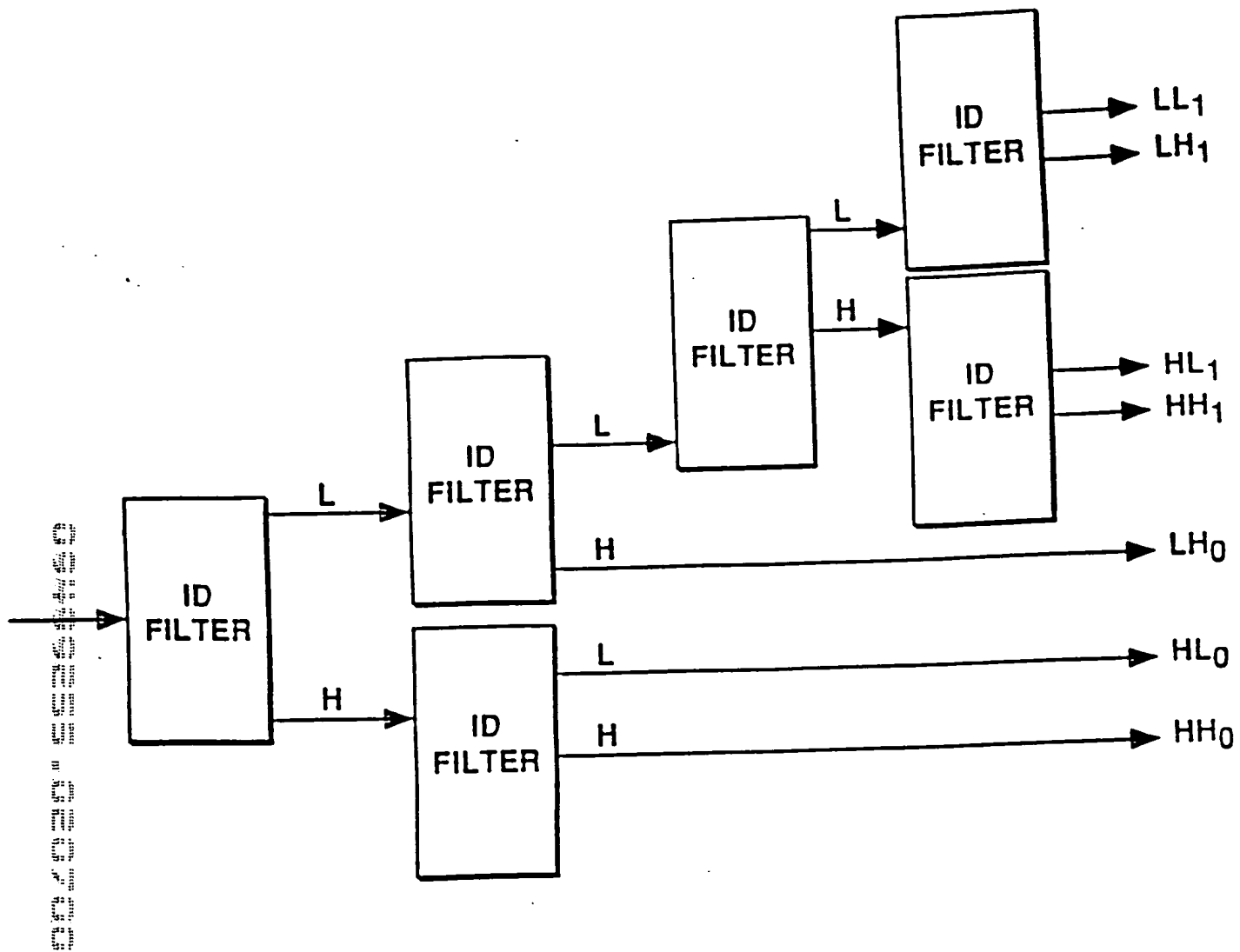


Figure 8



*Figure 9*

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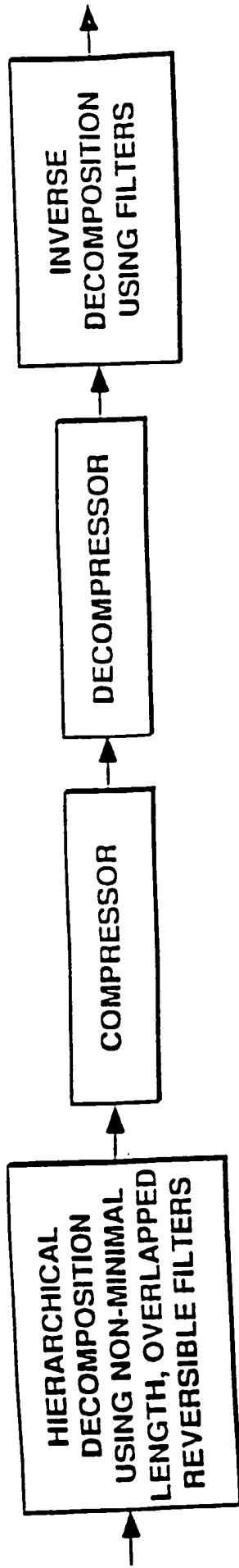


Figure 10

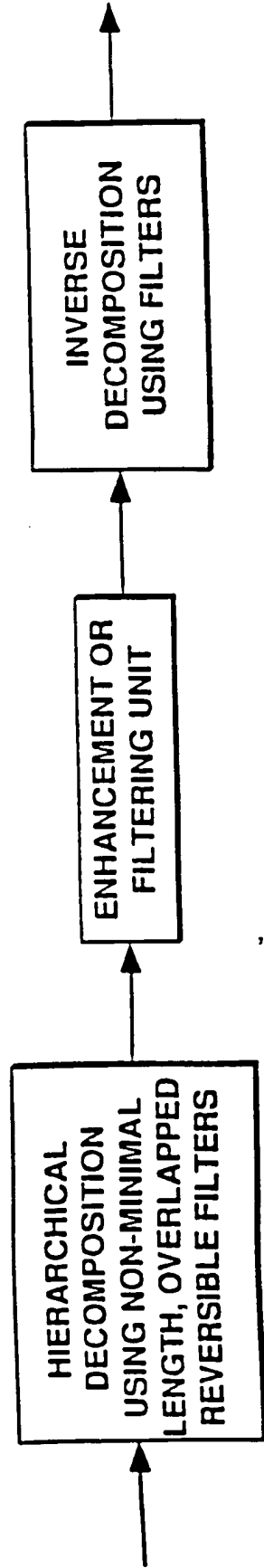
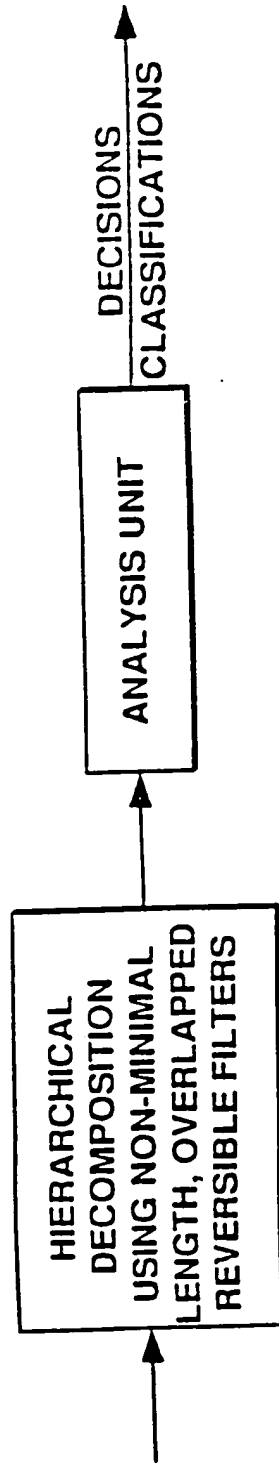


Figure 11

$b$	$b+2$	$b+2$
$b+2$	$b+4$	
$b+2$		$b+4$

Figure 12A

	16			
16	8	8		
	8	4	4	
			2	2
		4	2	
			2	1

FIGURE 123



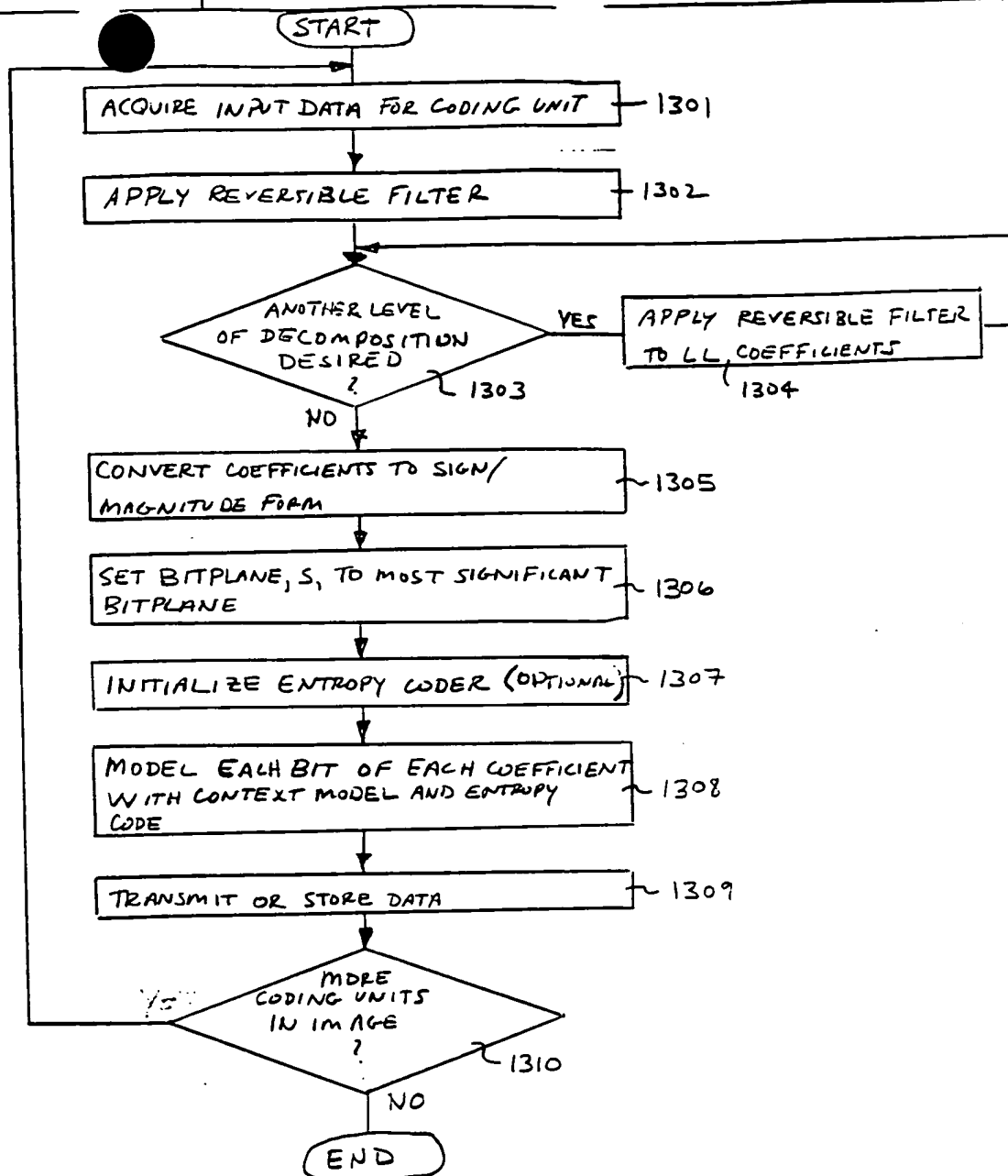


FIGURE 13

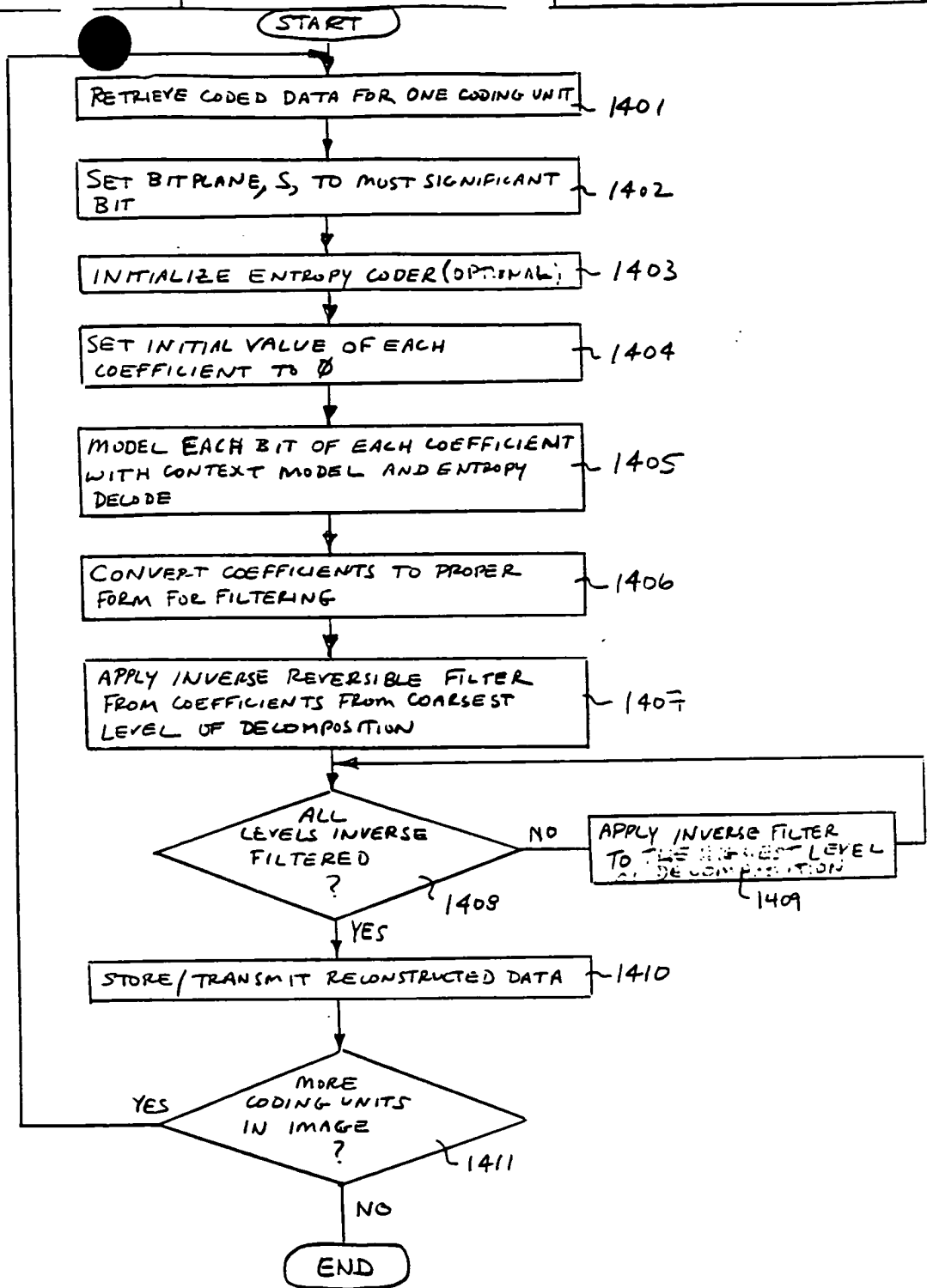
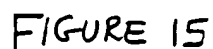


FIGURE 14



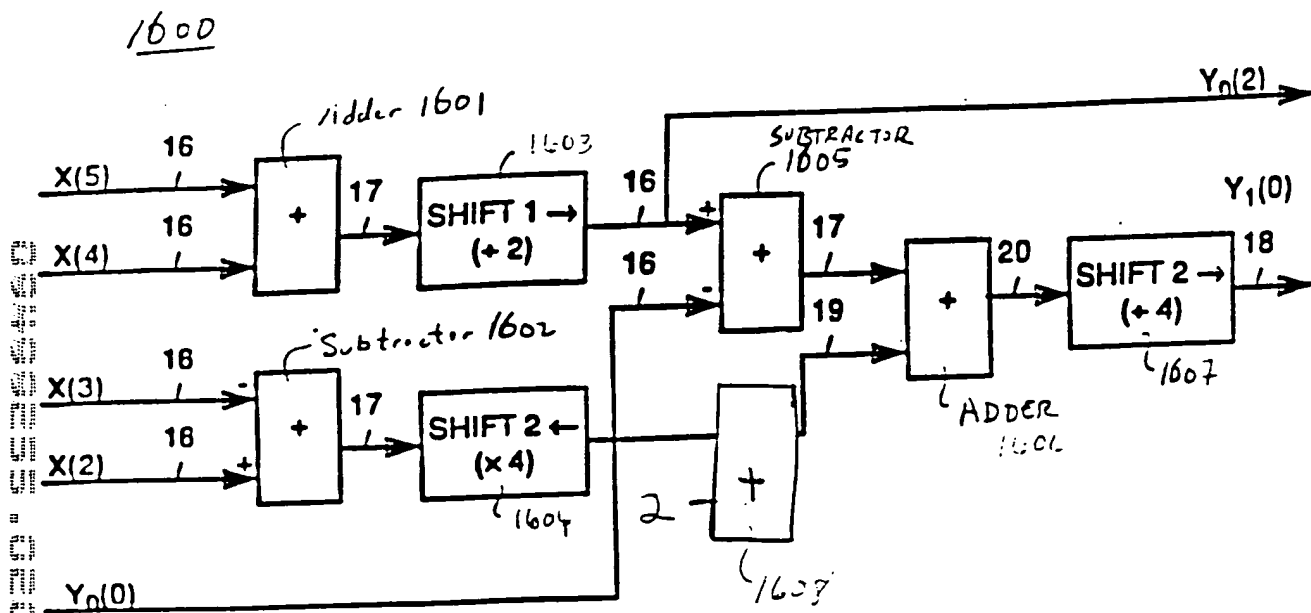


FIGURE 16

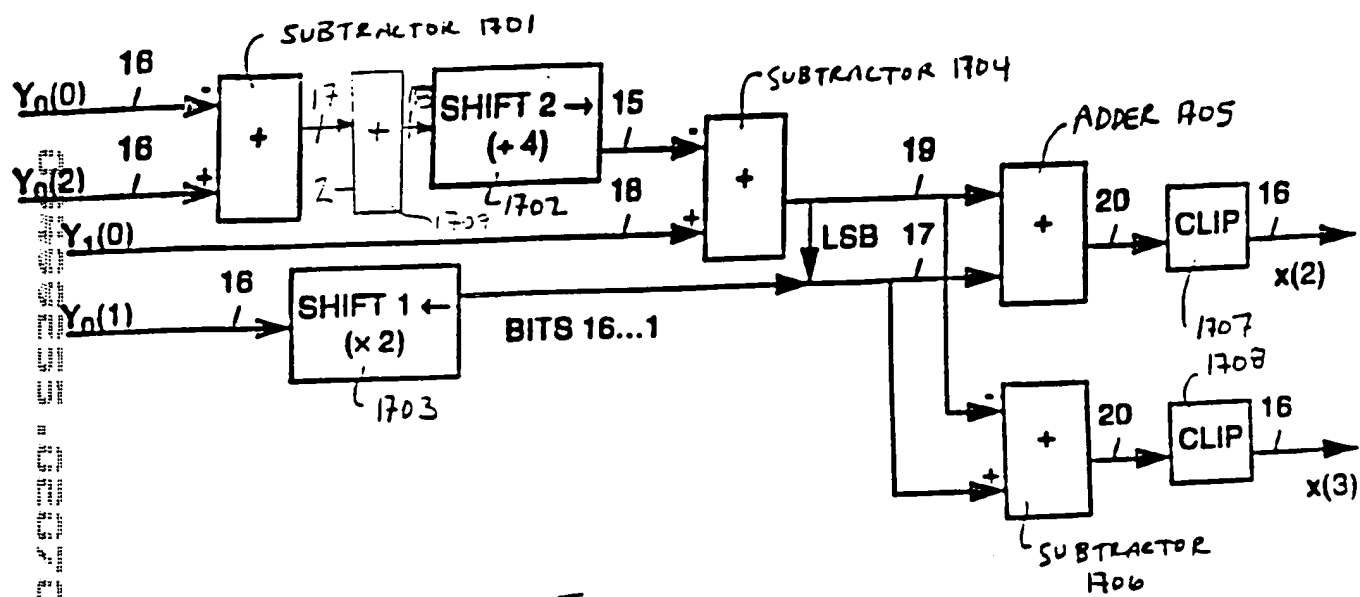


FIGURE 17

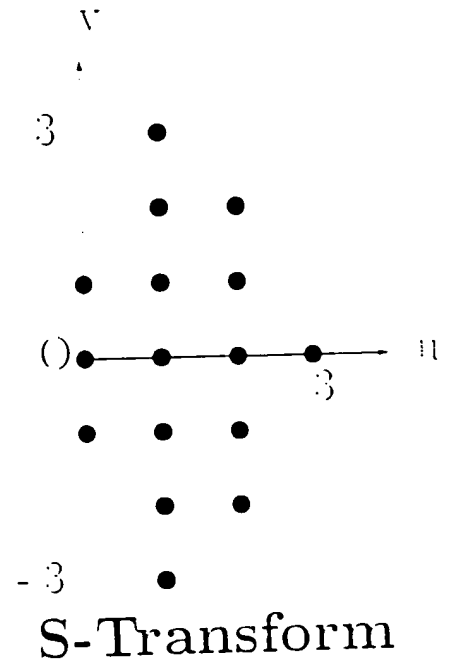
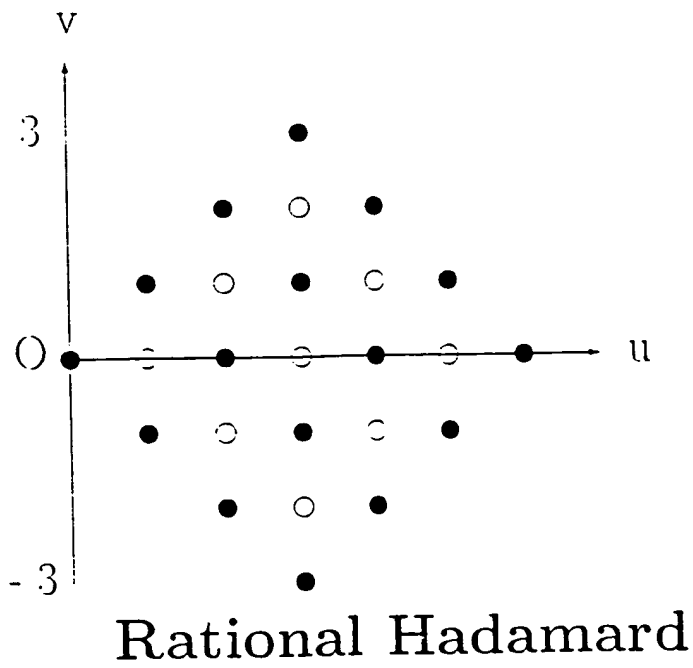
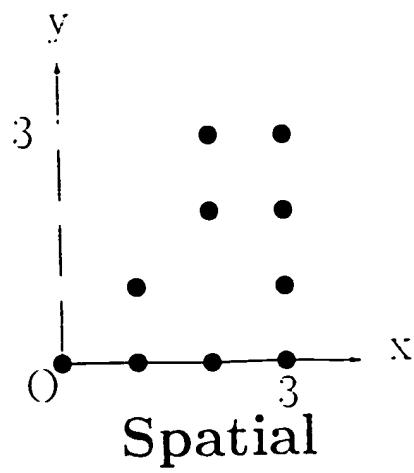


Figure 18

conditioning  
handled by LUT

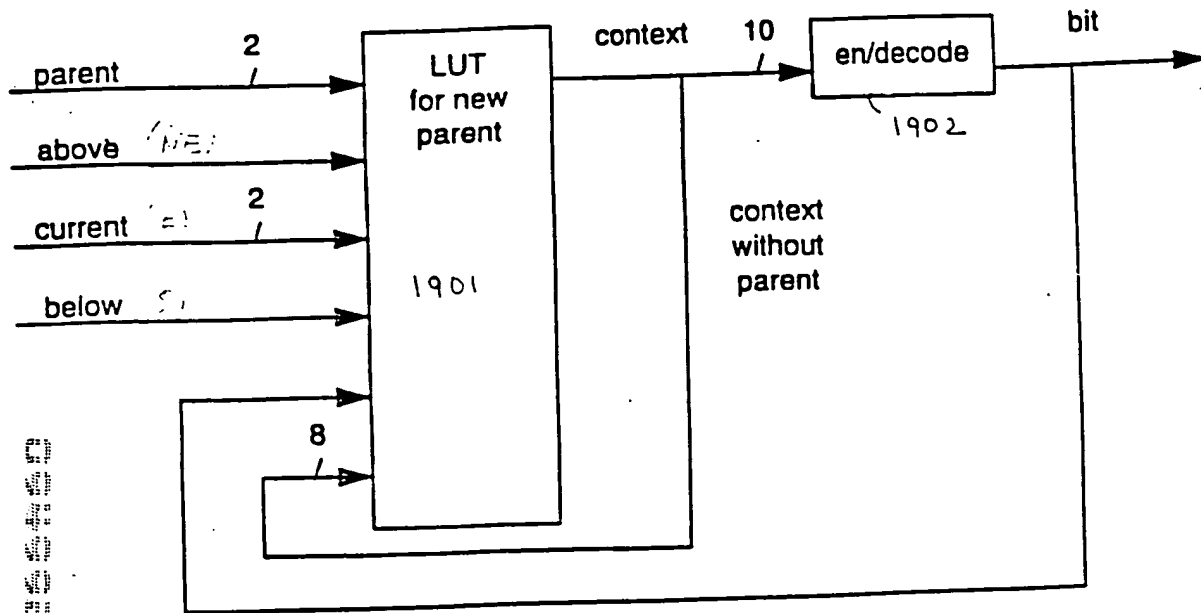
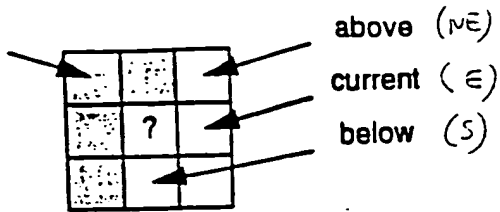


Figure 19A

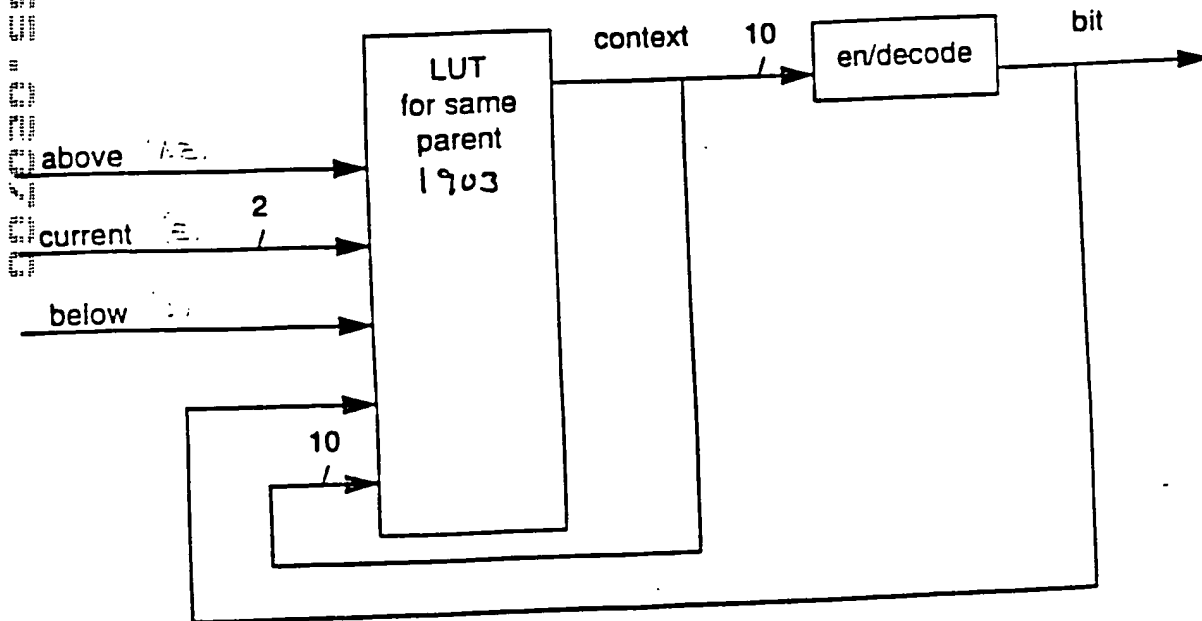


Figure 19B

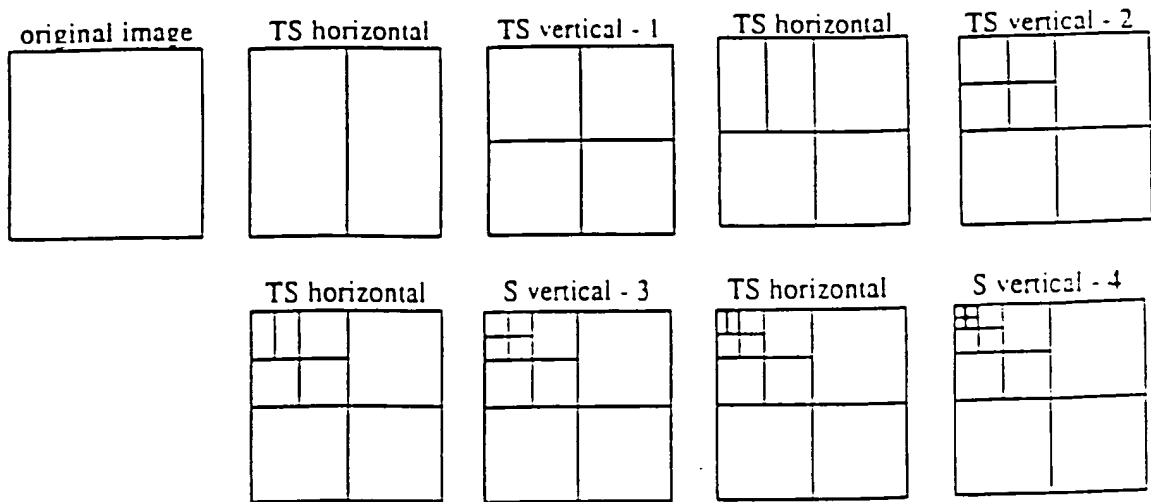
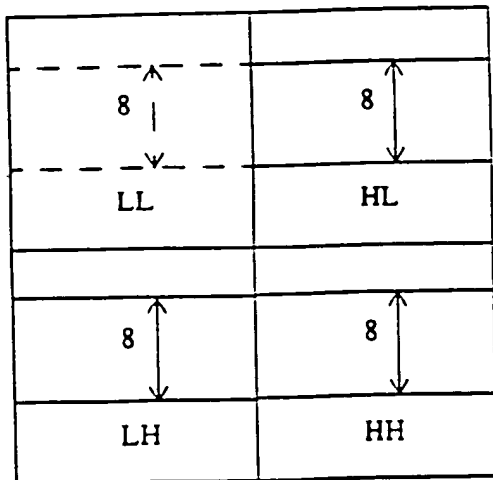
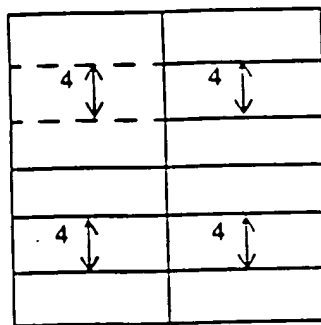


Figure 20





LEVEL 1



LEVEL 2



LEVEL 3



LEVEL 4

Figure 21

16 lines  
12 lines  
8 lines  
4 lines

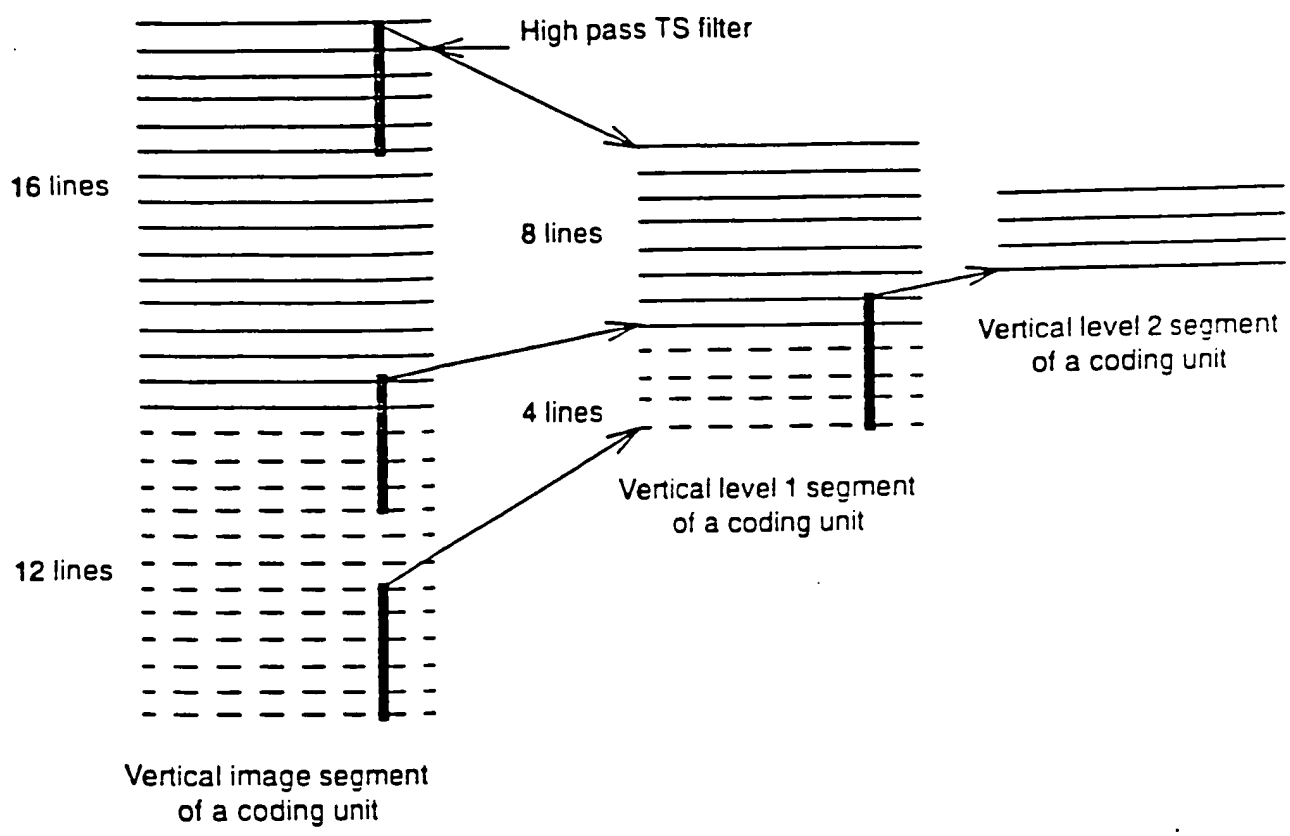
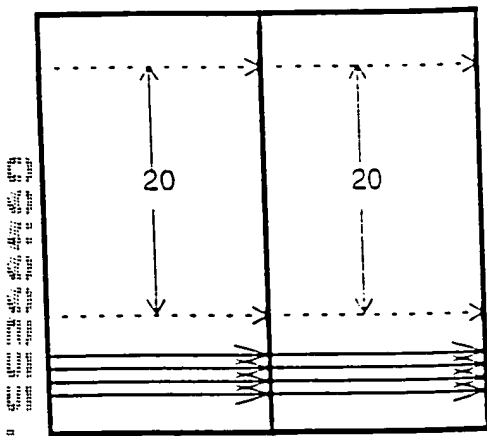
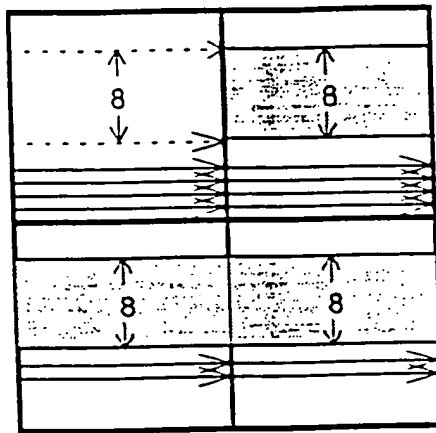


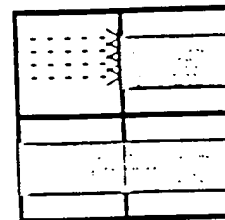
Figure 22



Level 0 (horizontal transform)



Level 1



Level 2

Vertical  
low pass

Vertical  
high pass

Figure 23

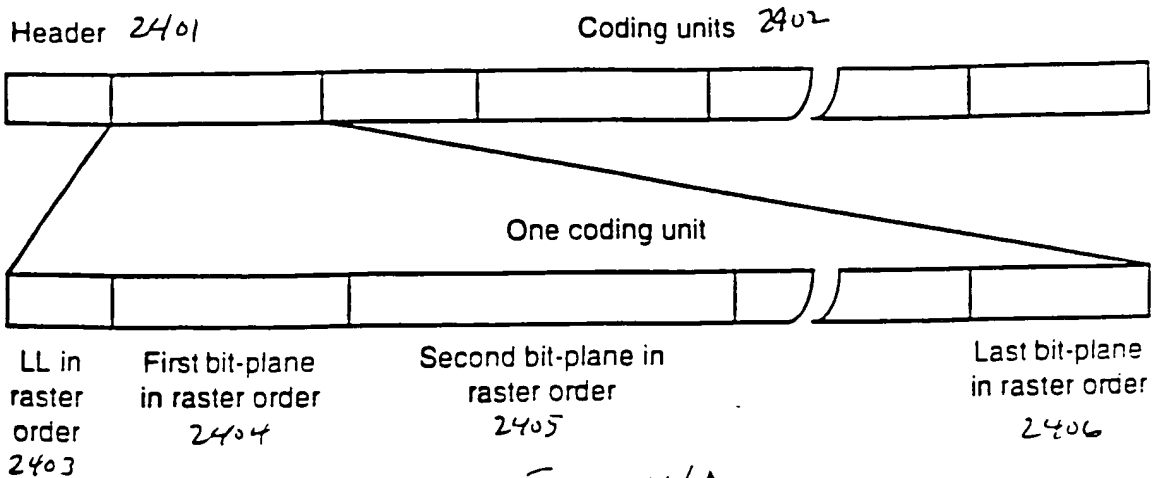


Figure 24A

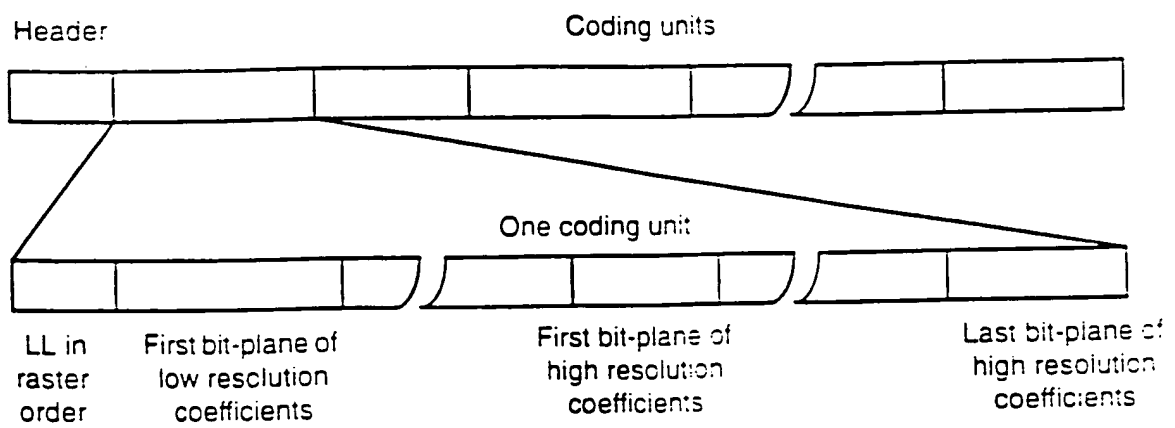
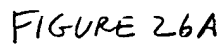


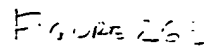
Figure 2-B

NW	N	NE
W	P	E
SW	S	SE

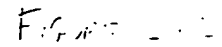
Figure 25



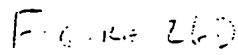
C



10



$C = \text{tail-on information (2 bits)}$



2700

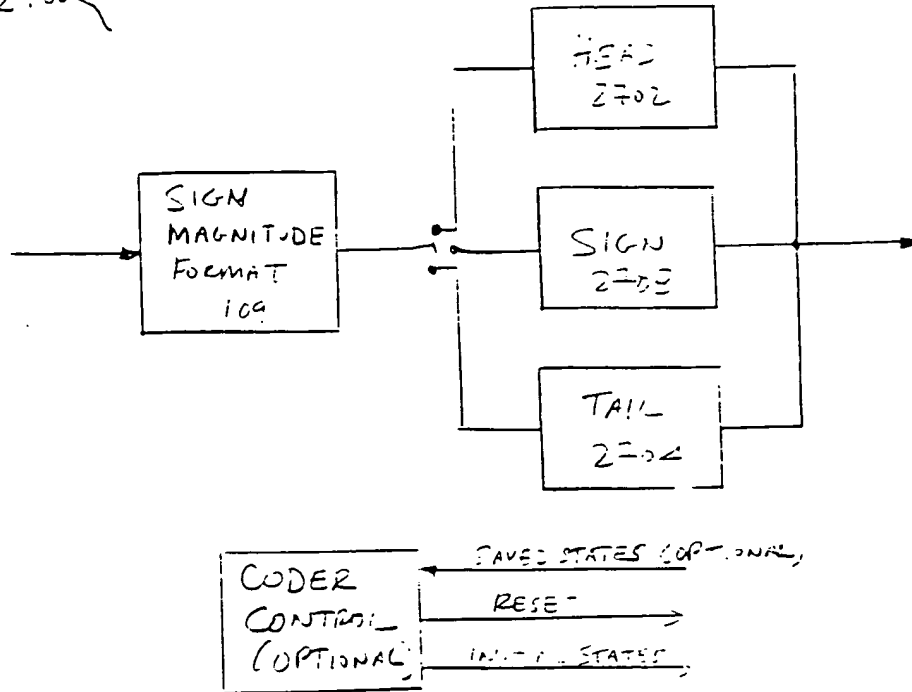


Figure 27



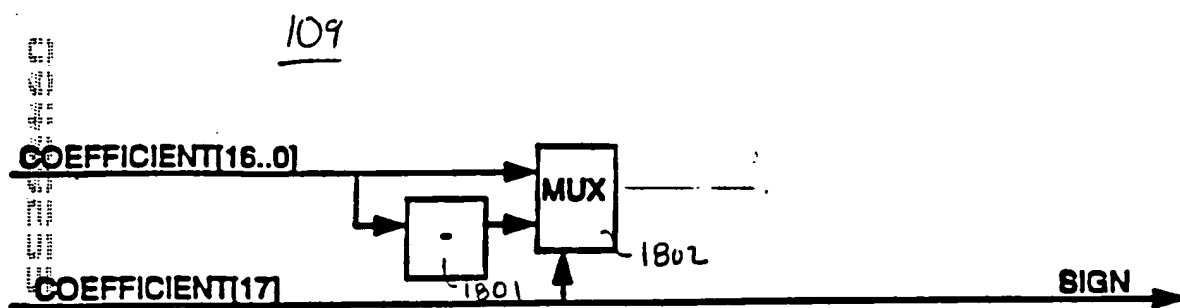


Figure 28

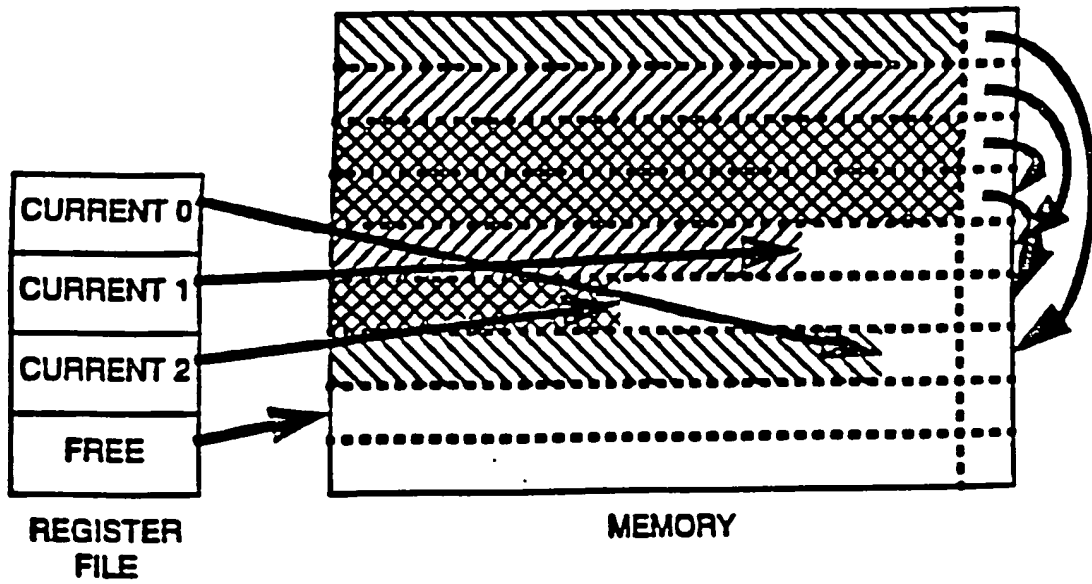


Figure 29

FIG. 30 is a block diagram of a system for processing data. The system includes a Wavelet Transform block (3001), a Context Model block (3002), a Channel Manager block (3003), and an Output Channel block (3004). The Wavelet Transform block (3001) is connected to the Context Model block (3002), which is connected to the Channel Manager block (3003). The Channel Manager block (3003) is connected to the Output Channel block (3004). The Channel Manager block (3003) also includes a Buffer Memory block (3003) and is connected to the Output Channel block (3004) via a Limited Bandwidth connection.

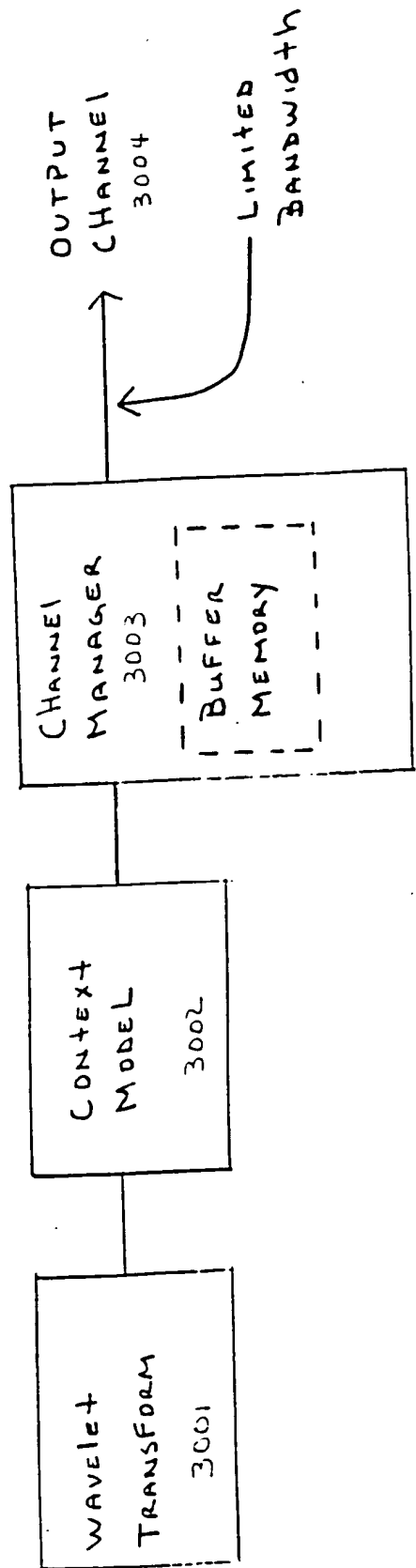


Figure 30

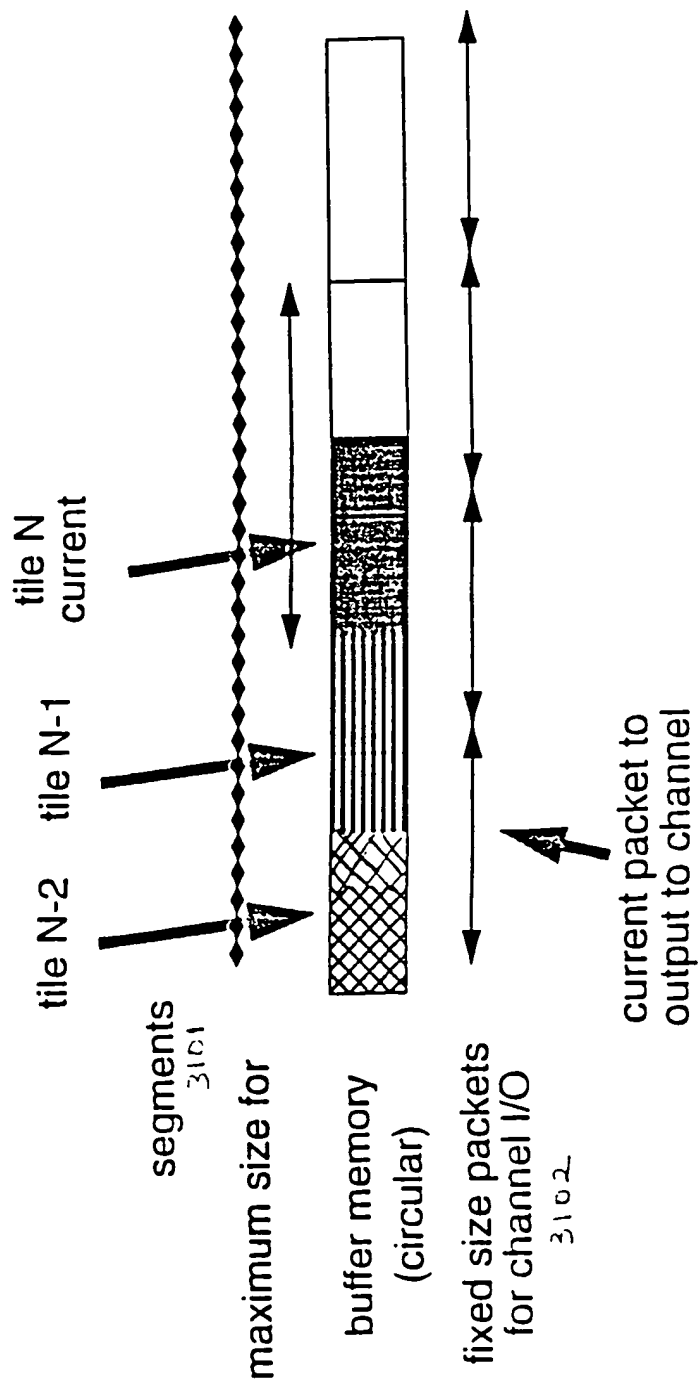


Figure 31

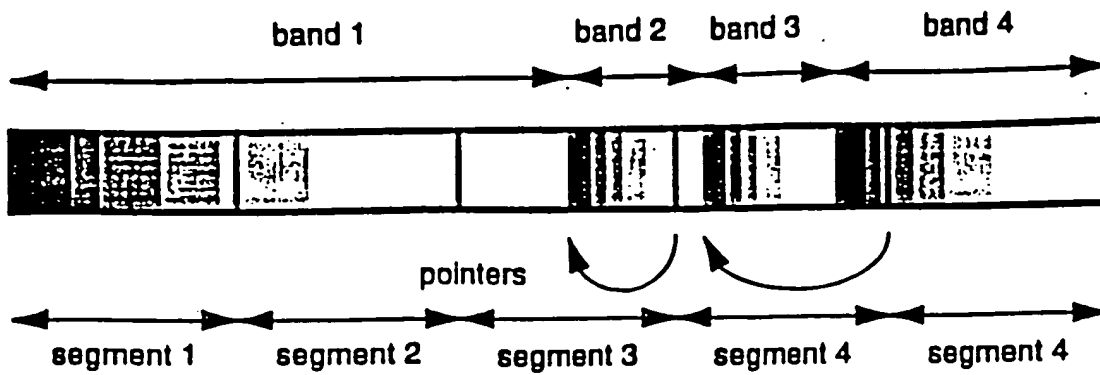


FIGURE 32

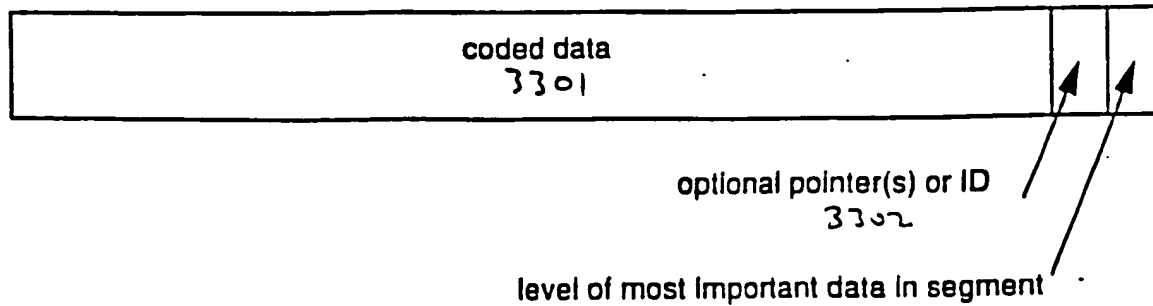


Figure 33

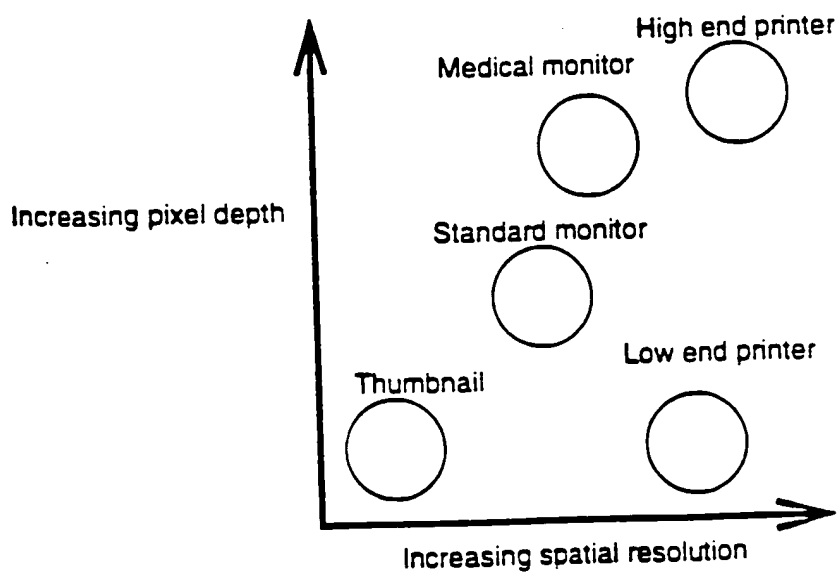
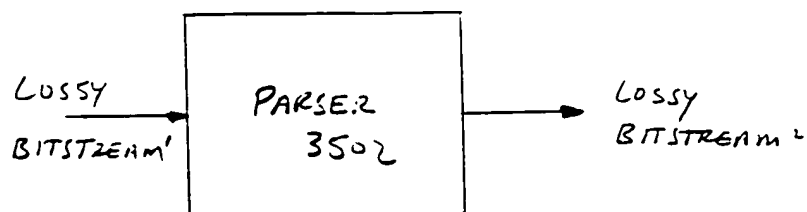
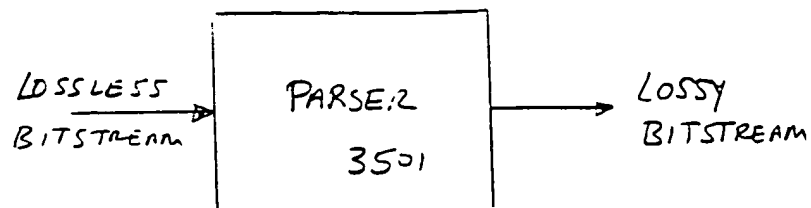


FIGURE 34



$\text{BITRATE} > \text{BITRATE}$

Figure 35